R18

Code No: 153AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, September/October - 2023

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT, ECM, ITE, CE(SE), CSE(CS), CSE(N))

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Define Ideal diode and practical diode.	[2]
b)	Explain the basic principle operation of an LED.	[3]
c)	What are the reasons for using multi-stage CE amplifiers?	[2]
d)	What is thermal runaway in the context of transistors, and why is it a concern in amplifier design?	[3]
e)	What does JFET stand for, and what type of transistor is it?	[2]
f)	Compare various logic families in terms of their characteristics and applications.	[3]
g)	List the applications of decoders.	[2]
h)	Which are universal gates? Why they called so?	[3]
i)	What is an excitation table? Draw the excitation table for SR Flip Flop.	[2]
j)	Describe the concept of state reduction in sequential circuit design.	[3]

PART – B

(50 Marks)

2. Define clipper and explain any '3' types of clippers. With the help of input and output wave forms and transfer characteristics. [10]

OR

3. Explain tunnel diode operation with the help of energy band diagrams. [10]

4. What is meant by bias compensation? Explain Diode Compensation Techniques. [10]

OR

5. Describe the operating principle of an emitter follower amplifier. How does it differ from a CE amplifier in terms of input and output characteristics? [10]

6. Describe the Common Source (CS) amplifier configuration. What are its key characteristics, and how does it provide voltage amplification? [10]

OR

7. Explain the operation of 3-input DTL NAND and NOR gates in detail. [10]

8. Design a 4-input priority encoder. [10]

OR

9. Find minimum sum of product form of the given function F(A,B,C,D) = ∑(1,3,5,6,7,12,14,15)+d(2,8,9) using K-Map and realize the circuit using NAND gates. [10]

10. Explain the operation of JK Flip flop and T-flip-flop with their characteristic tables. [10]

OR

11. Design a 4-bit asynchronous BCD counter using JK FF's. [10]

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